Impacts of Random Telegraph Noise (RTN) on Digital Circuits

Mulong Luo, Runsheng Wang, *Member, IEEE*, Shaofeng Guo, *Student Member, IEEE*, Jing Wang, Jibin Zou, *Student Member, IEEE*, and Ru Huang, *Senior Member, IEEE*

***Abstract*— Random telegraph noise (RTN) is one of the important dynamic variation sources in ultrascaled MOSFETs. In this paper, the recently focused ac trap effects of RTN in digital circuits and their impacts on circuit performance are systematically investigated. Instead of trap occupancy probability under dc bias condition (p_{dc}), which is traditionally used for RTN characterization, ac trap occupancy probability (p_{ac}), i.e., the effective percentage of time trap being occupied under ac bias condition, is proposed and evaluated analytically to investigate the dynamic trapping/detrapping behavior of RTN. A simulation approach that fully integrates the dynamic properties of ac trap effects is presented for accurate simulation of RTN in digital circuits. The impacts of RTN on digital circuit performances, e.g., failure probabilities of SRAM cells and jitters of ring oscillators, are then evaluated by the simulations and verified against predictions based on p_{ac}. The results show that degradations are highly workload dependent and that p_{ac} is critical in accurately evaluating the RTN-induced performance degradation and variability. The results are helpful for robust and resilient circuit design.**

***Index Terms*— Bit error rate (BER), dynamic variability, failure probability, Monte Carlo simulation, oxide trap, random telegraph noise (RTN), ring oscillator, signal integrity, SRAM.**

I. Introduction

RECENTLY, random telegraph noise (RTN) in nanoscale CMOS technology has attracted growing attention due to its increasing amplitude as the device scaling down [1]–[7]. RTN is one of the important dynamic variation sources in MOSFETs that the current fluctuating randomly between several discrete stages within a broad range of timescale [7]. It is believed that RTN is caused by the stochastic trapping/detrapping behavior of the channel carrier into the switching oxide traps (or border traps) in the gate dielectrics [7], [8].

Since RTN is due to the random trapping/detrapping fluctuations, it is important to study the RTN chronological statistics, including capture/emission time constants and trap occupancy probability, i.e., the average percentage of the total time the trap in trapping state. The chronological statistics of RTN are strongly dependent on working conditions of the device in the circuit. It has been found recently that the chronological statistics of RTN in device under ac large signal excitation, which we denote as ac RTN [9]–[13], is different from conventionally studied RTN under constant bias (dc RTN). Fig. 1(a) shows the typical experimental result of RTN under dc and ac conditions. It can be observed that the capture/emission time constants and trap occupancy probability are different under dc and ac workloads with different frequencies. Fig. 1(b) shows the extracted capture/emission time constant as a function of the ac frequency. The results show that, the capture time constant τ_c has no observable frequency dependence due to the fact that capture process during the low-phase ($V_G = 0$ V) of the ac signal is rare, while the emission time constant τ_e reduces with increasing frequency. Fig. 1(c) further plots the ac RTN trap occupancy probability versus frequency. Apparently, the trap occupancy probability is in negative correlation with the frequency of the ac signals (more specific discussions on frequency dependency will be explained in the following sections). All these phenomena will affect circuit operations and should be considered in circuit analysis [14]–[24].

In digital circuits, the RTN chronological statistics, especially the trap occupancy probability, have direct impacts on circuit performance, as the degradation like jitter of signals happens when the trap is occupied. Several works have been dedicated to the dc RTN statistics, but a more detailed

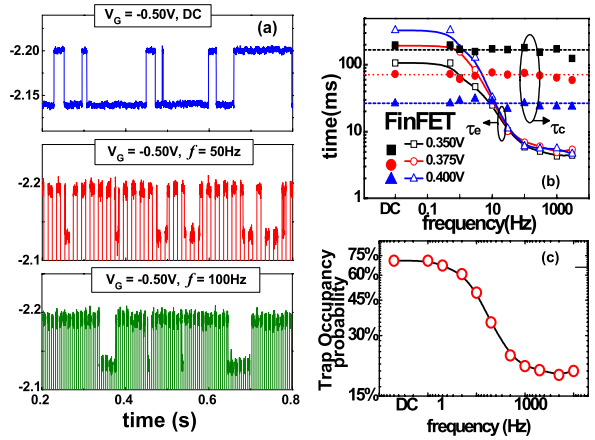

Fig. 1. (a) Typical measured data of dc and ac RTN in a PMOSFET, the excitation signal is between 0 and V_G for ac RTN. (b) Extracted time constants of ac RTN as a function of the ac excitation signal frequency in a FinFET device. (c) Extracted trap occupancy probability as a function of the ac signal frequency.

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The authors are with the Institute of Microelectronics, Peking University, Beijing 100871, China (e-mail: ruhuang@pku.edu.cn; r.wang@pku.edu.cn).

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RTN analysis with special attention to the ac effects has not been focused. Moreover, the impacts of the RTN statistics on different types of digital circuits should be systematically studied.

Therefore, in this paper, the RTN behavior in digital circuits and the impacts on circuit performance are comprehensively investigated. First, the chronological statistics considering the ac effects is studied analytically. Then, a simulation method for RTN in digital circuit is proposed, which is capable of accurately reconstructing the ac effects of RTN in simulations. Using this method, the impacts of RTN statistics on typical digital circuits including ring oscillator (RO) and SRAM cell are evaluated quantitatively and explained by the RTN statistics.

II. Understanding RTN in Digital Circuits

Traditionally, the statistics of RTN under dc bias is focused, which can be simply characterized by the capture/emission time constant under constant dc voltage. However, in digital circuits where the MOSFETs switch between ON state (VDD) and OFF state (GND), RTN statistics are actually determined by the capture/emission time constants of both ON state and OFF state [9], [10]. As shown in Fig. 2(a), capture/emission time constants in the OFF state and ON state are different due to the voltage dependence. The smaller emission time and larger capture time at OFF state makes the emission process more faster, which pulls down the transient trap occupancy probability at the end of the OFF state (p_1). As a result the effective trap occupancy probability during the whole ON state under ac conditions ($p_{\rm ac}$) reduces from that under dc conditions ($p_{\rm dc} = p_{\rm ON}$), as shown in Fig. 2(b).

To analytically express the trap occupancy probability during ON state under ac conditions, continuous-time Markov Chain is used [25]. Capture and emission time constants in the ON and OFF state are denoted as $\tau_{c\rm ON}$, $\tau_{e\rm ON}$, $\tau_{c\rm OFF}$, and $\tau_{e\rm OFF}$, respectively. Let DF be the duty factor (or, duty cycle), T be the period of the ac signal. As the figure shows, the transient trap occupancy probability during ON phase ($0 \le t < {\rm DF}\cdot T$) increases from p_1 to p_2, and we have

$$p(t) = p_{\rm ON} + (p_1 - p_{\rm ON}) \times \exp\left(-\frac{t}{\tau_{\rm ON}}\right). \quad (1)$$

On the other hand, during the OFF phase (${\rm DF}\cdot T \le t < T$), we have

$$p(t) = p_{\rm OFF} + (p_2 - p_{\rm OFF}) \times \exp\left(-\frac{t - {\rm DF}\cdot T}{\tau_{\rm OFF}}\right) \quad (2)$$

where $p_{\rm ON}$, $p_{\rm OFF}$ are the dc trap occupancy probability in the ON and OFF state, respectively

$$p_{\rm ON} = \frac{\tau_{e\rm ON}}{\tau_{e\rm ON} + \tau_{c\rm ON}}, \quad p_{\rm OFF} = \frac{\tau_{e\rm OFF}}{\tau_{e\rm OFF} + \tau_{c\rm OFF}}. \quad (3)$$

In addition, $\tau_{\rm ON}$ and $\tau_{\rm OFF}$ are the characteristic time in the ON and OFF state, respectively

$$\tau_{\rm ON} = \frac{\tau_{e\rm ON}\tau_{c\rm ON}}{\tau_{e\rm ON} + \tau_{c\rm ON}}, \quad \tau_{\rm OFF} = \frac{\tau_{e\rm OFF}\tau_{c\rm OFF}}{\tau_{e\rm OFF} + \tau_{c\rm OFF}}. \quad (4)$$

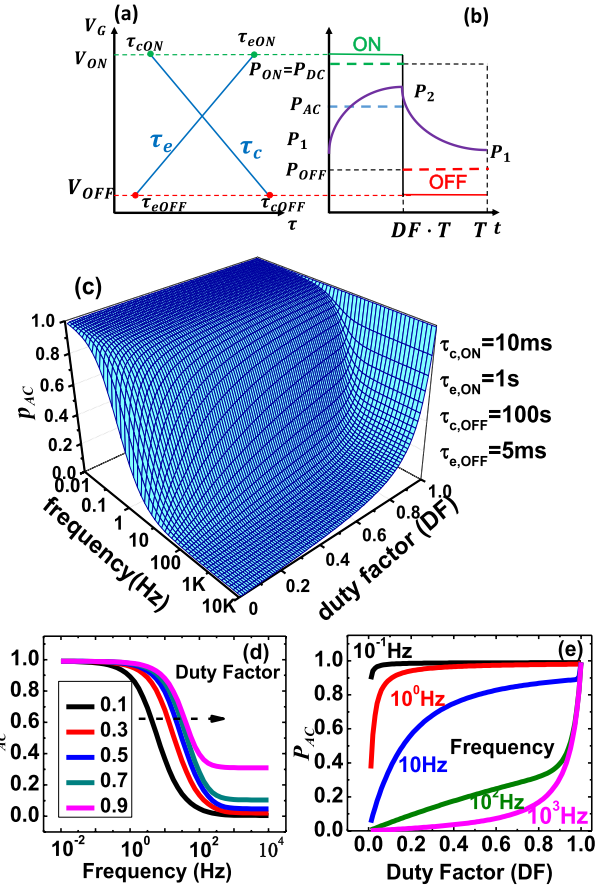


Fig. 2. (a) ON state ($V_G = V_{\rm ON}$) capture/emission time constant $\tau_{c\rm ON}$, $\tau_{e\rm ON}$ and OFF state ($V_G = V_{\rm OFF}$) capture/emission time constant $\tau_{c\rm OFF}$, $\tau_{e\rm OFF}$ are different due to the bias dependency of time constants. (b) Under ac large signal excitation with frequency f and duty factor (DF), the transient trap occupancy probability is periodically changed between p_1 and p_2, and the ac effective trap occupancy probability $p_{\rm ac}$ is between p_1 and p_2, which is different from $p_{\rm ON} = p_{\rm dc}$ under dc conditions. (c) Plot of the ac effective trap occupancy probability $p_{\rm ac}$ is a 2-D-function of ac excitation signal frequency and DF. (d) $p_{\rm ac}$ as functions of frequency under different DF. (e) $p_{\rm ac}$ as functions of DF under different frequency.

Due to the periodicity of the ac excitation, the transient trap occupancy probability $p(t)$ should follow the periodical boundary conditions:

$$p(0) = p(T), \quad p(({\rm DF}\cdot T)_-) = p(({\rm DF}\cdot T)_+). \quad (5)$$

In digital circuits, the effective trap occupancy probability is defined by the average trap occupancy probability in the ON state

$$p_{\rm ac} = \frac{1}{{\rm DF}\cdot T}\int_0^{{\rm DF}\cdot T} p(t)dt. \quad (6)$$

Using the above equations (1)–(4), one can calculate $p_{\rm ac}$, as a function of the frequency ($f = 1/T$), DF, $\tau_{c\rm ON}$, $\tau_{e\rm ON}$, $\tau_{c\rm OFF}$, and $\tau_{e\rm OFF}$.

Fig. 2(c) is a demonstration of $p_{\rm ac}$ as the 2-D function of frequency and DF of the ac signal. Fig. 2(d) and (e) further shows the intersactions of Fig. 2(c). They clearly show that: 1) $p_{\rm ac}$ decreases with the frequency under almost all DFs; 2) $p_{\rm ac}$ saturates and no longer changes with the frequency at high frequency (when the period of ac signal

is much smaller than the trap time constants); and 3) $p_{\rm ac}$ is less sensitive to the frequency under ac signal with higher duty cycle. The frequency dependence of the time constants described in Section I can be well understood here. The trap occupancy probability $p_{\rm ac}$ at a certain frequency f can be approximated by $\tau_e(f)/[\tau_c(f) + \tau_e(f)]$. Since τ_c has no frequency dependence, as $p_{\rm ac}$ decreases with increasing f, τ_e will decrease with it. These theoretical predictions are consistent with the experiments and are critical to evaluate the impact of ac RTN on circuits, as will be discussed in the following sections.

III. Circuit Simulation Approach

A. Compact Modeling of RTN

As mentioned in Section II, to accurately incorporating ac effects of RTN statistics into digital circuit simulation, the bias dependence of the capture/emission time constants under different biases should be carefully modeled. In addition, the amplitude model of the RTN under different bias is critical in predicting the impacts on digital circuits.

For the time constants model, we adopt [8]

$$\tau_c = \tau_0\left(1+\exp\left(-\frac{E_F-E_T}{kT}\right)\right) \tag{7}$$

$$\tau_e = \tau_0\left(1+\exp\left(\frac{E_F-E_T}{kT}\right)\right) \tag{8}$$

where τ_0, E_T, and E_F are the characteristic time constant of the trap, trap energy level, and the surface potential of the device, respectively. For single-trap-induced RTN, τ_0 and E_T have single values. If considering the statistics of large numbers of RTN in different devices, one should consider the trap distributions. For various traps in MOSFETs, τ_0 is found to be log-uniform distributed [26]–[29]. The distribution of E_T can be extracted from either theoretical simulation [7] or experiment [30]. For example, for simplicity, it can be assumed to be U-shape distributed in the bandgap [26]. The distribution is critical for statistical analysis in large-scale circuits with many devices of different trap configurations. The bias-dependent E_F can be calculated from the device core model like BSIM-CMG [31].

As for the amplitude of RTN typically characterized by $\Delta V_{\rm TH}$ or $\Delta I/I$, it is widely recognized that both of them are largely dependent on the gate voltage V_G, even though several efforts have been made to derive the analytical expression for the amplitude, some of the details are not fully incorporated. For example, hole-in-the-inversion-layer model only derives the maximum possible amplitude of RTN for different traps [4], regardless of the variations of the amplitude of RTN induced by different traps. Recent advances in atomistic simulation and fast characterization [6] give a possible solution for the amplitude model. While in subthreshold region $\Delta V_{\rm TH}$ distribute widely for different devices, they converge near $2\eta_0$ in the ON-state, where $\eta_0 = q/C_{\rm ox}$ and q, $C_{\rm ox}$ is the unit charge and gate oxide capacitance, respectively [6]. The behavior of this gate overdrive dependence can be explained by the channel percolation theory. In subthreshold region, the percolation currents domains and a single trap is capable of causing large variations of RTN amplitude based on the profile of the trap. On the other hand, in strong inversion, the drain current is dominated by the sheet current and the variations of $\Delta V_{\rm TH}$ induced by traps tend to be small. Therefore, the apparent threshold voltage shift could be effectively taken as a function of the voltage of transistor. For circuit simulation convenience, we adopt a piecewise voltage controlled voltage source (VCVS) $\Delta V_{\rm TH}$ model shown in Fig. 3

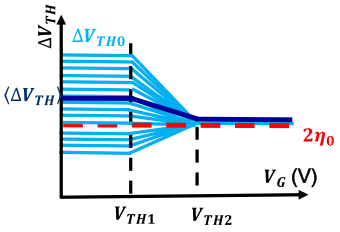


Fig. 3. Schematic of the amplitude model of RTN used in this paper. For different traps, the amplitude of a single-trap-induced RTN (light blue line) distribute widely in the subthreshold region but in the ON-state the amplitudes distribute much closer to its ideal value (red dashed line). However, the average amplitude (dark blue line) of all traps decrease within the transition region.

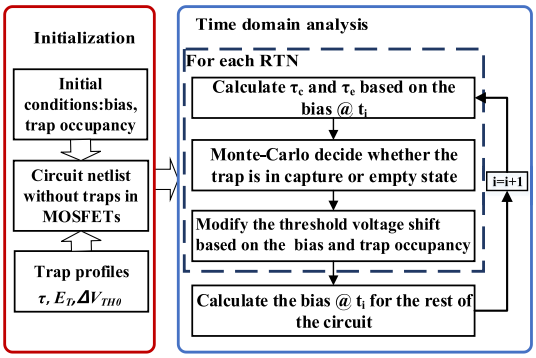


Fig. 4. Flowchart of the circuit simulation presented in this paper.

$$\Delta V_{\rm TH} = \begin{cases} \Delta V_{\rm TH0}, & V_{\rm GS} \le V_{\rm TH1} \\ (V_{\rm GS}-V_{\rm TH1}) \times \frac{2\eta_0-\Delta V_{\rm TH0}}{V_{\rm VH2}-V_{\rm TH1}} + \Delta V_{\rm TH0}, & V_{\rm TH1} < V_{\rm GS} < V_{\rm TH2} \\ 2\eta_0, & V_{\rm GS} \ge V_{\rm TH2} \end{cases} \tag{9}$$

where $V_{\rm TH1}, V_{\rm TH2}$ are the boundaries of the transition from the subthreshold region to the fully ON state region. $\Delta V_{\rm TH0}$ is usually found to be exponentially distributed for different traps [26], [29], [32]. In general, $V_{\rm TH1}, V_{\rm TH2}$, and η_0 can be calibrated from experiments or from theoretical simulations [6].

B. Monte Carlo Simulation Methodology

With the time constants and amplitude models, we are able to simulate RTN behavior in digital circuits using SPICE simulator. Based on our newly proposed method [33], the flowchart of the simulation is shown in Fig. 4. First, we initialize the simulation by setting RTN trap profiles and initial conditions of the circuits and trap occupancy. The initialized values are then put in time domain analysis. In the first step of the time domain analysis, we calculate the

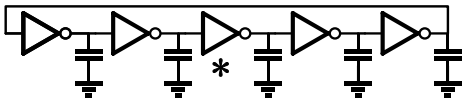


Fig. 5. Five-stage RO with RTN on the nMOS of one stage (denoted with an asterisk). The capacitor is connected between the output of each stage and ground to model fan-out of the logic gates.

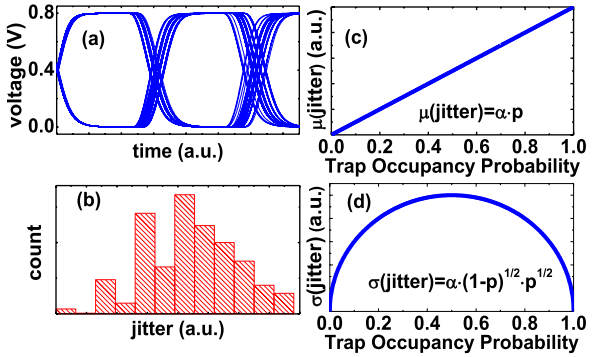


Fig. 6. (a) Eye diagram of the signal in typical logic circuits. Due to RTN, the delay in each cycle is not a constant value. (b) Histogram of the RTN-induced jitter, due to RTN, the jitter distributes in a range rather than at single value. (c) Average jitter of signal induced by a particular trap is proportional to the trap occupancy probability. (d) Variation of the jitter of the signal follows a quadratic relationship with the trap occupancy probability.

capture/emission probability based on the time constants of the traps, in the second step we Monte Carlo decide whether capture/emission will happen, in the third step the threshold voltage is modified based on bias and trapping occupancy. A variable is used to mark the trap occupancy.

Then in the final step, the biases of the rest of the circuit are calculated. The process is repeated for every time point the until the last time point.

Due to generating RTN during the SPICE simulation in this flow rather than predetermining the RTN waveform before SPICE simulation, the impacts of bias in circuits on the statistics of RTN can be accurately incorporated. On the other hand, the RTN-induced threshold voltage shift is immediately applied in each loop. With both directions carefully modeled, the complex interactions and feedbacks between RTN waveforms and circuits bias that may happen in real digital circuits can precisely simulated.

IV. Impacts on Typical Digital Circuits

In the following analysis, we focus on the single RTN cases, that is only one RTN/trap exists in one device in the circuit, to make a primary understanding of the relations from RTN profile to circuit performance. The device used in circuit simulations is 16-nm double-gate bulk FinFET with the Fin height and width as 18 and 8 nm, respectively.

A. RO Signal Integrity

For evaluation of the impact of RTN on combinational logical circuits, we adopt signal integrity analysis and take a five-stage RO for demonstrations as shown in Fig. 5.

Fig. 6(a) and (b) shows the eye diagram of a RO and its respective jitter obtained from statistical SPICE simulations.

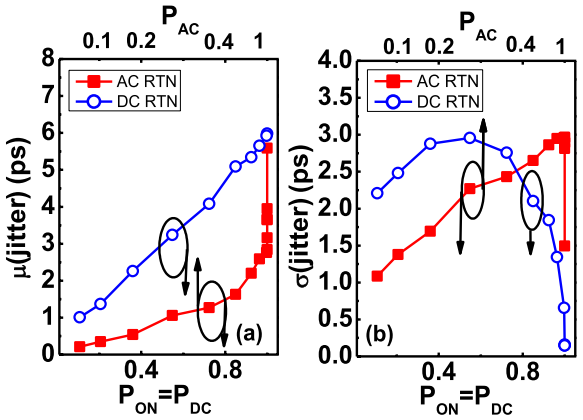


Fig. 7. (a) and (b) μ(jitter) and σ(jitter), respectively, of RO with dc/ac RTN effects as functions of their respective dc/ac trap occupancy probability.

As shown in Fig. 6(a), the jitter of signal in RO varies from cycle to cycle, which is due to the stochastic RTN events in the MOSFETs of the logic gates. Fig. 6(b) plots the distribution of the jitter induced by RTN. As RTN is a random process, its impact on the signal integrity is a function of its statistical quantities rather than transient ones. Assume the occupied state of a trap during the whole RO period will cause an extra delay α, thus the average jitter μ(jitter) for a signal is proportional to the percentage of the time that the trap being occupied, i.e., the effective trap occupancy probability ($p_{\rm dc}$ or $p_{\rm ac}$) in Section II

$$\mu(\text{jitter}) = \alpha \cdot p. \tag{10}$$

In addition, the standard deviation of the jitter follows:

$$\sigma(\text{jitter}) = \sqrt{(0-\mu(\text{jitter}))^2(1-p) + (\alpha-\mu(\text{jitter}))^2 \cdot p}. \tag{11}$$

Taking (10) into (11) we get

$$\sigma(\text{jitter}) = \alpha \cdot \sqrt{(1-p)\cdot p}. \tag{12}$$

Fig. 6(c) and (d) shows the μ(jitter) and σ(jitter) as a function of the trap occupancy probability. As the figures show, while μ(jitter) is monotonous with p, the σ(jitter) follows a nonmonotonous trend, which increase when $p < 0.5$ but decrease when $p > 0.5$. According to signal integrity theory, broader distribution of the jitter can lead to higher bit error rate (BER) because extra jitter may lead to the total delay in the critical path outside the timing slack and causing a bit error. In other words, BER of the circuits my increase even if the trap occupancy probability is reduced. Note that (10) and (12) are just predictions of circuit performance based on the proposed theory in Section II. We will see that they match the result of statistical SPICE simulations well.

Fig. 7 is the simulation results of μ(jitter) and σ(jitter) of the RO as a function dc effective trap occupancy probability and the respective ac effective trap occupancy probability. To get a better approach of the real circuit operations, we have set the total simulation time much longer than the trap time constants to get stable distribution of the jitter. The simulation

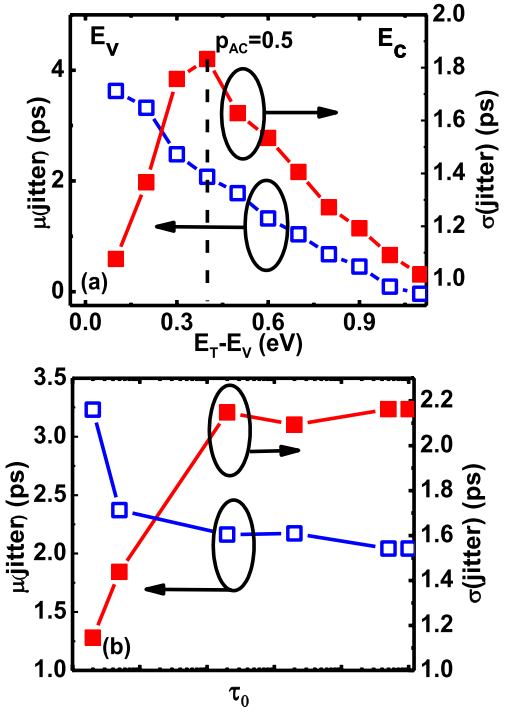


Fig. 8. (a) and (b) μ(jitter) and σ(jitter), respectively, of RO as a function of trap energy level τ_0.

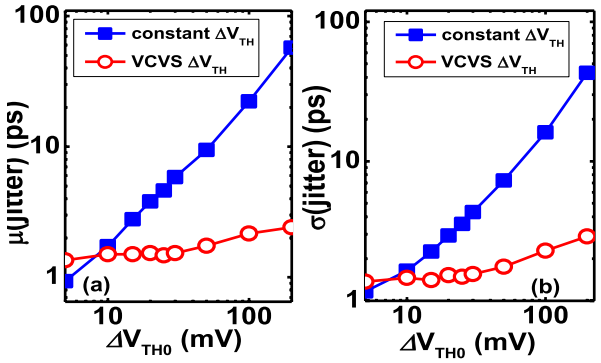


Fig. 9. (a) and (b) μ(jitter) and σ(jitter), respectively, of RO as a function of the amplitude of RTN. Both the results of VCVS $\Delta V_{\rm TH}$ model and constant $\Delta V_{\rm TH}$ model are presented.

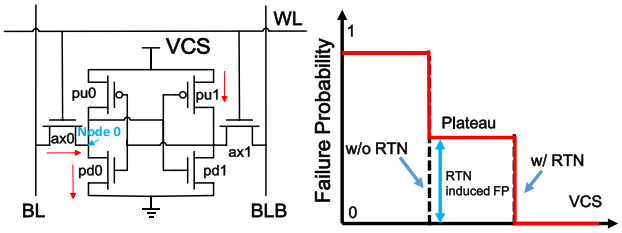


Fig. 10. (a) Schematic of SRAM, RTN is assumed to be presented in one of the nMOS. (b) Failure probability-VCS curve of SRAM with and without RTN.

results of not considering the ac effects of RTN (i.e., dc RTN) are also plotted for reference. From the figure we can see that dc RTN and its dc effective trap occupancy probability $p_{\rm dc}$ roughly follows (10) and (12). For ac RTN, large deviation from dc case is observed, which is due to the reduction of effective trap occupancy probability under ac conditions from dc conditions. On the other hand, ac RTN still roughly follows (10) and (12) if using $p_{\rm ac}$ instead of $p_{\rm dc}$. This implies that $p_{\rm ac}$ is critical in predicting circuits performance and that we should take the ac effects into account in circuit performance evaluation.

To take a closer look at how the ac RTN impacts combinational circuits for different traps, we draw μ(jitter) and σ(jitter) of the RO against RTN parameters. Fig. 8(a) shows the relationship of μ(jitter) and σ(jitter) with the trap energy level E_T. Based on (6)–(8), lower trap level in terms of electron energy will lead to higher trap occupancy probability. Thus, larger μ(jitter) is observed when the trap level is closer to the valence band. With the trap energy level moves from E_V to E_C, the respective effective trap occupancy probability rises from 0 to 1 continuously. In this process, there will be a particular energy level whose corresponding trap occupancy probability is 0.5. At this energy, the σ(jitter) got its maximum value. On the other hand, when the trap energy level is close to conduction or valence band, the trap will be always empty or occupied, thus the σ(jitter) is much smaller under this condition.

Fig. 8(b) shows the μ(jitter) and σ(jitter) against τ_0. The μ(jitter) reduces and σ(jitter) increases with the increase of τ_0, both saturates at large τ_0. This can be understood from the observations in Section II. As τ_0 increases, the reflection of trap to excitations become slower compared with the ac signal frequency, leading to reduction of trap occupancy probability $p_{\rm ac}$, as discussed above. According to (10) and (12), due to the lower $p_{\rm ac}$, the average jitter induced by RTN decreases, whereas, the σ(jitter) increases probably due that $p_{\rm ac}$ is between 1 and 0.5 in this case, thus in negative relation with σ(jitter). The simulation results are also in consistency with the experimental observations of trap occupancy probability in Section I.

Another important feature that should be paid attention is the bias (especially gate overdrive) dependence of the amplitude of ac RTN. As has been mentioned above, trap-induced $\Delta V_{\rm TH}$ turns from $\Delta V_{\rm TH0}$, which is widely distributed for different devices in the subthreshold region to $2\eta_0$ in the ON-state. In Fig. 9, we plot the average μ(jitter) and σ(jitter) of the RO with RTN against $\Delta V_{\rm TH0}$, the results of adopting simple constant ΔV_{TH}model, which has been widely used before, are also shown in the same figures for reference. In both cases, μ(jitter) and σ(jitter) are in positive relevance with the amplitude. However, large reduction of both μ(jitter) and σ (jitter) are observed from the results of simple constant $\Delta V_{\rm TH}$ model to accurate VCVS $\Delta V_{\rm TH}$ model, which is due to the overestimation of the RTN amplitude within the full swing range of the signals by the simple constant $\Delta V_{\rm TH}$ model.

B. SRAM Cell Stability

Fig. 10(a) shows the structure of 6-T SRAM cell and Fig. 10(b) plots the transient read failure probability against VCS. A plateau is presented in the read failure probability when considering RTN. As RTN in the transistor changes

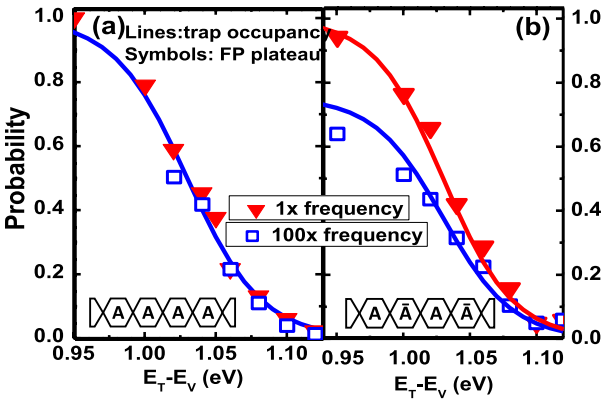


Fig. 11. Simulation results of the RTN-induced SRAM failure probability of two types of read-after-write patterns and respective trap occupancy probability. (a) Pattern 1: write the same logic 0 in every cycle, p_{dc} is plotted for reference (blue line). (b) Pattern 2: switch the value written in the following cycle. p_{ac} under original frequency (red line) and 100× original frequency (blue line) are plotted for reference.

the current, the noise margin of SRAM is changed, thus the minimum supply voltage for passing the operation will be a different value when the trap is occupied as shown in the figure. One the other hand, the trap occupancy probability of observable RTN is a non-0-or-1 value for RTN, thus a non-0-or-1 plateau between minimum supply voltage when considering RTN effects.

To accurately mapping SRAM failure probability to RTN statistics, a typical case that RTN is only presented in pd0 is focused in the following demonstrations. During read, the transistor will discharge the capacitor connected to BL and GND (not shown in the figure). Because RTN reduce the current of the pull down transistor, the voltage of Node 0 will possibly be switched from prestored logic 0 (GND) to logic 1 (VCS) during read, and thus a read failure happens.

Differently from RO, which is constantly switching between ON and OFF state, the bias of transistors in the cell is in fact based on the pattern of read, write, and the value stored in the SRAM cell. We study two typical patterns in read-after-write cycles shown in Fig. 11. Pattern 1: write the same logic value in every read-after-write cycles. Pattern 2: switch the values written in the read-after-write cycles next to each other. In Pattern 1 the pd0 is constantly biased in the ON-state, whereas in Pattern 2 pd0 is continuously switching between ON and OFF state. Due to the different workload of pd0, the statistics of RTN in that device will be different. As consequence, the failure probabilities of reading logic zero (GND) in Node 0 are different under the two patterns.

Fig. 11(a) shows the height of the plateau in the failure probability-VCS plot of Pattern 1. In both frequencies, the failure probability is close to $p_{ON} = p_{dc}$, which ascertain the dc RTN nature in pd0 under this pattern. However, when using the Pattern 2, large reduction of failure probability is observed under higher frequency [Fig. 11(b)], which fits the p_{ac} calculated from (1)–(6).

Fig. 12 further shows failure probability against frequency under Pattern 2. The figure ascertains the observation that failure probability reduces as the frequency goes up. p_{ac} as

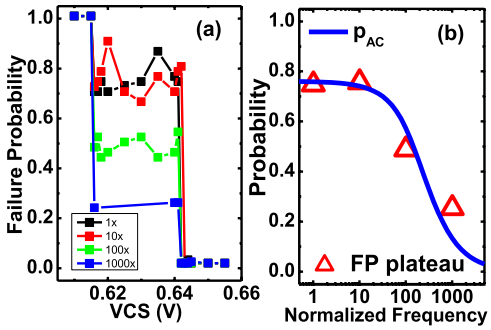


Fig. 12. (a) Simulated SRAM failure probability of Pattern 2 due to RTN under different frequencies. (b) Simulated failure probability plateau height of Pattern 2 against frequency, p_{ac} is also plotted for reference.

a function of frequency is also plotted in Fig. 12(b). From all these observations above it is clear that the height of the failure probability plateau is roughly equal to p_{ac} of ac RTN in pd0.

As the simulation result shows, the failure probability of SRAM could be inferred from the effective trap occupancy probability, which is related to its read/write pattern. In practical applications, the read/write pattern of SRAM is not a periodical pattern like Pattern 1 or Pattern 2, but the value would be switched somehow in real patterns, which could be regarded as a mixture of Pattern 1 and Pattern 2. Thus, the failure probability induced by RTN would also have frequency dependencies.

On the other hand, it seems that for certain cases (e.g., the scale of RTN time constants is much smaller than ac signal period), the adoption of dc RTN as a metric might not cause much difference for this particular single RTN case. However, in reality since the time constants of various RTN is widely distributed on a log scale for different traps [26]–[29], the safe frequency range to use dc RTN as metrics will be different for different traps. Thus, it can hardly guarantee that all the traps in real applications are at their safe frequency. Therefore, simply using dc RTN will cause deviations in most cases for practical digital circuit operations.

V. Conclusion

In this paper, the recently focused ac effects of RTN in digital circuits and their impacts on circuit performance are systematically investigated. The effective trap occupancy probability under ac conditions p_{ac} is proposed instead of p_{dc} to characterize RTN in circuits and calculated analytically. A simulation approach that fully integrates ac effects into SPICE simulations is presented and implemented to evaluate the impact of RTN on digital circuits. The results show that average jitter of RO is smaller than dc RTN if taking ac effects into consideration, while the change of variation of jitter have two tendencies based on p_{ac} of that RTN. For SRAM, it is found that the failure probability decreases when the value of the pattern is switched and that failure probability under real patterns decreases with frequency, which is consistent with the prediction by p_{ac}. The results are helpful for the RTN aware robust and resilient circuit design.

REFERENCES

[1] H. Miki *et al.*, "Statistical measurement of random telegraph noise and its impact in scaled-down high-*k*/metal-gate MOSFETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 19.1.1–19.1.4.

[2] H. Miki *et al.*, "Voltage and temperature dependence of random telegraph noise in highly scaled HKMG ETSOI nFETs and its impact on logic delay uncertainty," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2012, pp. 137–138.

[3] S. Realov and K. L. Shepard, "Random telegraph noise in 45-nm CMOS: Analysis using an on-chip test and measurement system," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2010, pp. 28.2.1–28.2.4.

[4] R. G. Southwick *et al.*, "Physical model for random telegraph noise amplitudes and implications," in *Proc. IEEE Silicon Nanoelectron. Workshop (SNW)*, Jun. 2012, pp. 1–2.

[5] J. Chen, Y. Higashi, I. Hirano, and Y. Mitani, "Experimental study of channel doping concentration impacts on random telegraph signal noise and successful noise suppression by strain induced mobility enhancement," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2013, pp. T184–T185.

[6] J. Franco *et al.*, "Impact of single charged gate oxide defects on the performance and scaling of nanoscaled FETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2012, pp. 5A.4.1–5A.4.6.

[7] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectron. Rel.*, vol. 52, no. 1, pp. 39–70, 2012.

[8] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (I/*f*) noise," *Adv. Phys.*, vol. 38, no. 4, pp. 367–468, 1989.

[9] J. Zou *et al.*, "New insights into AC RTN in scaled high-*k*/metal-gate MOSFETs under digital circuit operations," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2012, pp. 139–140.

[10] J. Zou *et al.*, "Deep understanding of AC RTN in MuGFETs through new characterization method and impacts on logic circuits," in *Proc. VLSI Symp. Technol. (VLSIT)*, Jun. 2013, pp. T186–T187.

[11] A. P. van der Wel, E. A. M. Klumperink, L. K. J. Vandamme, and B. Nauta, "Modeling random telegraph noise under switched bias conditions using cyclostationary RTS noise," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1378–1384, May 2003.

[12] J. S. Kolhatkar *et al.*, "Modeling of RTS noise in MOSFETs under steady-state and large-signal excitation," in *IEEE Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 2004, pp. 759–762.

[13] N. Zanolla, D. Siprak, M. Tiebout, P. Baumgartner, E. Sangiorgi, and C. Fiegna, "Reduction of RTS noise in small-area MOSFETs under switched bias conditions and forward substrate bias," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 1119–1128, May 2010.

[14] A. P. van der Wel *et al.*, "Low-frequency noise phenomena in switched MOSFETs," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 540–550, Mar. 2007.

[15] T. Matsumoto, K. Kobayashi, and H. Onodera, "Impact of random telegraph noise on CMOS logic delay uncertainty under low voltage operation," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 25.6.1–25.6.4.

[16] K. Ito, T. Matsumoto, S. Nishizawa, H. Sunagawa, K. Kobayashi, and H. Onodera, "Modeling of random telegraph noise under circuit operation—Simulation and measurement of RTN-induced delay fluctuation," in *Proc. 12th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2011, pp. 1–6.

[17] G. Wirth, D. Vasileska, N. Ashraf, L. Brusamarello, R. D. Giustina, and P. Srinivasan, "Compact modeling and simulation of random telegraph noise under non-stationary conditions in the presence of random dopants," *Microelectron. Rel.*, vol. 52, no. 12, pp. 2955–2961, 2012.

[18] H. Luo, Y. Wang, Y. Cao, Y. Xie, Y. Ma, and H. Yang, "Temporal performance degradation under RTN: Evaluation and mitigation for nanoscale circuits," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI)*, Aug. 2012, pp. 183–188.

[19] Q. Tang, X. Wang, J. Keane, and C. H. Kim, "RTN induced frequency shift measurements using a ring oscillator based circuit," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2013, pp. T188–T189.

[20] M.-L. Fan, V. P.-H. Hu, Y.-N. Chen, S. Pin, and C.-T. Chuang, "Impacts of random telegraph noise on FinFET devices, 6T SRAM cell, and logic circuits," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2012, pp. CR.1.1–CR.1.6.

[21] Y. Ye, C.-C. Wang, and Y. Cao, "Simulation of random telegraph noise with 2-stage equivalent circuit," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 709–713.

[22] K. Takeuchi *et al.*, "Direct observation of RTN-induced SRAM failure by accelerated testing and its application to product reliability assessment," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2010, pp. 189–190.

[23] K. Aadithya, S. Venogopalan, A. Demir, and J. Roychowdhury, "MUSTARD: A coupled, stochastic/deterministic, discrete/continuous technique for predicting the impact of random telegraph noise on SRAMs and DRAMs," in *Proc. 48th ACM/EDAC/IEEE Design Autom. Conf. (DAC)*, Jun. 2011, pp. 292–297.

[24] M. Yamaoka *et al.*, "Evaluation methodology for random telegraph noise effects in SRAM arrays," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 32.2.1–32.2.4.

[25] S. Karlin and H. M. Taylor, *A First Course in Stochastic Processes*. New York, NY, USA: Academic, 1975, pp. 474–502.

[26] G. I. Wirth, R. da Silva, and B. Kaczer, "Statistical model for MOSFET bias temperature instability component due to charge trapping," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2743–2751, Aug. 2011.

[27] J.-P. Chiu, Y.-H. Liu, H.-D. Hsieh, C.-W. Li, M.-C. Chen, and T. Wang, "Statistical characterization and modeling of the temporal evolutions of ΔV_t distribution in NBTI recovery in nanometer MOSFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 978–984, Mar. 2013.

[28] T. Nagumo, K. Takeuchi, T. Hase, and Y. Hayashi, "Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps," in *Proc. IEEE IEDM*, Dec. 2010, pp. 628–631.

[29] T. Grasser, K. Rott, H. Reisinger, M. Waltl, J. Franco, and B. Kaczer, "A unified perspective of RTN and BTI," in *Proc. IEEE IRPS*, Jun. 2014, pp. 4A.5.1–4A.5.7.

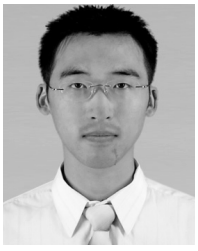
[30] P. Ren *et al.*, "New insights into the design for end-of-life variability of NBTI in scaled high-*k*/metal-gate technology for the nano-reliability era," in *IEDM Tech. Dig.*, 2014.

[31] *BSIM-CMG: Multi-Gate MOSFET Compact Model*. [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/, accessed 2012.

[32] K. Takeuchi, T. Nagumo, S. Yokogawa, K. Imai, and Y. Hayashi, "Single-charge-based modeling of transistor characteristics fluctuations based on statistical measurement of RTN amplitude," in *Proc. Int. Symp. VLSI Technol. (VLSI)*, Jun. 2009, pp. 54–55.

[33] R. Wang *et al.*, "A unified approach for trap-aware device/circuit co-design in nanoscale CMOS technology," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 834–837.

Mulong Luo received the B.S. degree in microelectronics from Peking University, Beijing, China, in 2014. He is currently pursuing the Ph.D. degree with the Department of Computer Science and Engineering, University of California at San Diego, La Jolla, CA, USA.



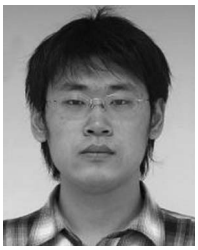
Runsheng Wang (S'07–M'11) received the Ph.D. degree in microelectronics from Peking University, Beijing, China, in 2010.

He is currently an Associate Professor with the Institute of Microelectronics, Peking University.

Dr. Wang was a recipient of the 2013 IEEE Electron Devices Society Early Career Award.

Shaofeng Guo (S'13) received the B.S. degree in microelectronics from Jilin University, Changchun, China, in 2011, and the M.S. degree in microelectronics from Peking University, Beijing, China, in 2014, where he is currently pursuing the Ph.D. degree with the Institute of Microelectronics.

Jing Wang is currently pursuing the B.S. degree with the Institute of Microelectronics, Peking University, Beijing, China.



Jibin Zou (S'11) received the B.S. and Ph.D. degrees in microelectronics from Peking University, Beijing, China, in 2009 and 2014, respectively.

He is currently with Oracle, Redwood City, CA, USA.

Ru Huang (M'98–SM'06) received the Ph.D. degree in microelectronics from Peking University, Beijing, China, in 1997.

She is currently a Professor and the Director of the Institute of Microelectronics with Peking University.